

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	203	instruction adj set adj simulator	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 15:57
L2	14	1 and microcontroller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:51
L3	5806	microcontroller and simulat\$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:52
L4	60	microcontroller and simulation.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:52
L5	6	4 and ((test adj bench) or stimulus)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:55
L6	0	("8051" adj3 simulation) and markers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:56
L7	1	("8051" same simulation) and markers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:56
L8	6	(microcontroller same simulation) and markers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 17:46
L9	361	(703/22).CCLS.	USPAT	OR	OFF	2005/06/16 17:46

L10	8	9 and microcontroller	USPAT	OR	OFF	2005/06/16 17:48
L11	7	10 and clock	USPAT	OR	OFF	2005/06/16 17:48
L12	11	("5103394" "5604895" "5613098" "5671352" "5680584" "5745767").PN. OR ("6223144").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/16 17:49

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The MC9S12DP256B **microcontroller simulation** runs in Single Chip modes. ...

Instruction timing is emulated. The 68HCS12 **simulator** will run Motorola's D-Bug12 ...

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A microcontroller course using a **simulator-based lab** would be restricted to ...

What is needed to **set up** an Advanced Microcontroller Laboratory is a ...

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Place and ... Basic parts of a Computer: ISA (**Instruction Set Architecture**), ...

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Gearold R. Johnson, Robert A. Mueller

 March 1976 **ACM SIGPLAN Notices , Proceedings of the ACM SIGMINI/SIGPLAN interface meeting on Programming systems in the small processor environment**, Volume 11 Issue 4

 Full text available: [pdf \(783.32 KB\)](#) Additional Information: full citation, abstract, references, index terms

ASM/GEN and SIM/GEN are a software system comprised of a set of independent FORTRAN program writer modules designed to generate micro computer and small minicomputer assemblers and simulators. It is simple enough to be used by those with limited architecture and programming backgrounds, but flexible and powerful enough to generate efficient and well-structured assemblers and simulators for small micro/minicomputers with sophisticated architectures and instruction sets. This paper presents ...

2 [Combining theorem proving and trajectory evaluation in an industrial environment](#)

Mark D. Aagaard, Robert B. Jones, Carl-Johan H. Seger

 May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

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We describe the verification of the IM: a large, complex (12,000 gates and 1100 latches) circuit that detects and marks the boundaries between Intel architecture (IA-32) instructions. We verified an agate-level model of the IM against an implementation-independent specification of IA-32 instruction lengths. We used theorem proving to derive 56 model-checking runs and to verify that the model-checking runs imply that the IM meets the specification for all possible sequences of IA-32 instructions. Our v ...

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